What is claimed is:

1. A memory cell of a semiconductor device, comprising:

a substrate having active regions and field regions;

a gate layer formed over the substrate, the gate layer including a plurality of access gates formed over the active regions of the substrate and a plurality of pass gates formed over the field regions of the substrate;

first self-aligned contact regions **(BC SAC region)** formed between adjacent pass gates and access gates; and

second self-aligned contact regions **(DC SAC region)** formed between adjacent access gates,

wherein a width of each of the first self-aligned contact regions is larger than a width of each of the second self-aligned contact regions.

2. The memory cell of a semiconductor device as claimed in claim 1, wherein the width of each of the first self-aligned contact regions is made larger than the width of each of the second self-aligned contact regions by each one of the plurality of access gates having a width smaller than a width of an adjacent pass gate.

3. The memory cell of a semiconductor device as claimed in claim 1, wherein a ratio of the width of the first self-aligned contact region to the width of the second self-aligned contact region is between about 1.0 to 1.2.

4. The memory cell of a semiconductor device as claimed in claim 3, wherein the ratio of the width of the first self-aligned contact region to the width of the second self-aligned contact region is about 1.1.

5. The memory cell of a semiconductor device as claimed in claim 1, further comprising:

sidewall spacers formed on sidewalls of each of the plurality of access gates and each of the plurality of pass gates.

6. The memory cell of a semiconductor device as claimed in claim 5, further comprising:

a recess hole having an opening and a bottom for receiving one of the plurality of access gates, wherein a width of the opening of the recess hole is larger than a width of the bottom of the recess hole.

7. The memory cell of a semiconductor device as claimed in claim 6, wherein the sidewall spacers formed on sidewalls of the plurality of access gates extend below an upper surface of the substrate.

8. The memory cell of a semiconductor device as claimed in claim 5, further comprising:

an interlayer dielectric layer formed over the sidewall spacer formed on the sidewall of one of the plurality of pass gates and the field region of the substrate.

9. The memory cell of a semiconductor device as claimed in claim 2, wherein the width of each of the plurality of access gates is

decreased by a notch formed on at least one side of each of the plurality of access gates.

10. The memory cell of a semiconductor device as claimed in claim 9, wherein the notch has a depth of between about 10 - 20 nm.

11. The memory cell of a semiconductor device as claimed in claim 9, wherein the notch formed on at least one side of each of the plurality of access gates is formed adjacent to the first self-aligned contact region so as to face one of the plurality of pass gates.

12. The memory cell of a semiconductor device as claimed in claim 9, wherein the notch formed on at least one side of each of the plurality of access gates is formed adjacent to the second self-aligned contact region so as to face one of the plurality of access gates.

13. The memory cell of a semiconductor device as claimed in claim 9, wherein each of the plurality of access gates has a pair of notches,

each notch formed on opposing sides of each of the plurality of access gates.

14. A method for forming a memory cell of a semiconductor memory device comprising:

forming an isolation region and an active region on a substrate;

performing an ion implantation to form a source/drain region in the substrate;

forming a recess gate hole by etching the substrate in the active region;

forming a gate oxide layer on the active region of the substrate;

forming a gate layer and a gate mask layer sequentially on the entire surface of the substrate; and

etching the gate layer and the gate mask layer to form a plurality of access gates on the active region of the substrate and a plurality of pass gates on the field region of the substrate and to form a notch in each of the plurality of access gates so that a width of each of the plurality of access gates is narrower than a width of each of the pass gates, to thereby form a first self-aligned contact region between adjacent pass gates and access gates and a second self-aligned contact region between adjacent access gates,

whereby a width of the first self-aligned contact region is larger than a width of the second self-aligned contact region.

15. The method for forming a memory cell of a semiconductor memory device as claimed in claim 14, further comprising:

forming sidewall spacers on sidewalls of each of the plurality of access gates and each of the plurality of pass gates.

16. The method for forming a memory cell of a semiconductor memory device as claimed in claim 14, wherein forming a recess gate hole by etching the substrate in the active region comprises:

etching the substrate to form a recess gate hole having an opening and a bottom, wherein a width of the opening of the recess hole is larger than a width of the bottom of the recess hole.

17. The method for forming a memory cell of a semiconductor memory device as claimed in claim 16, further comprising:

forming sidewall spacers on sidewalls of each of the plurality of access gates and each of the plurality of pass gates, wherein the sidewall spacers formed on sidewalls of the plurality of access gates extend below an upper surface of the substrate.

18. The method for forming a memory cell of a semiconductor memory device as claimed in claim 15, further comprising:

forming an interlayer dielectric layer over the sidewall spacer formed on the sidewall of one of the plurality of pass gates and the field region of the substrate.

19. The method for forming a memory cell of a semiconductor memory device as claimed in claim 14, wherein forming the notch comprises:

forming the notch on at least one side of each of the plurality of access gates adjacent to the first self-aligned contact region so as to face one of the plurality of pass gates.

20. The method for forming a memory cell of a semiconductor memory device as claimed in claim 14, wherein forming the notch comprises:

forming the notch on at least one side of each of the plurality of access gates adjacent to the second self-aligned contact region so as to face one of the plurality of access gates.

21. The method for forming a memory cell of a semiconductor memory device as claimed in claim 14, wherein forming the notch comprises:

forming a pair of notches in each of the plurality of access gates, each notch being formed on opposing sides of each of the plurality of access gates.